WHAT IS CLAIMED IS:

1. A phase-locked loop apparatus, comprising:

a comparator configured to compare phases of a reference clock signal and an output signal of said apparatus and to output a voltage in accordance with a difference in phase as a comparison result;

a filter configured to integrate the voltage output from said comparator;

a voltage-controlled oscillator configured to control a frequency of an output signal in accordance with the voltage output from said filter, said voltage-controlled oscillator comprising:

a ring oscillator configured to include a delay circuit including a plurality of inverters connected in a ring form;

a plurality of first transistors corresponding to said plurality of inverters of said ring oscillator on a one-to-one basis and configured to control a current supplied by a first power source voltage to a positive side power source terminal of each of said plurality of inverters;

a plurality of second transistors corresponding to said plurality of inverters of said ring oscillator on a one-to-one basis and configured to control a current output from a negative side power source terminal of each of said plurality of inverters;

a voltage-to-current converter configured to convert said voltage output from said filter into a current;

a first current mirror circuit configured to output a current in accordance with the current output from said voltage-to-current converter;

a second current mirror circuit configured to output a current in accordance with the current output from said first current mirror circuit to a control signal input terminal of each of said plurality of first transistors; and

a third current mirror circuit configured to output a current in accordance with the current output from said second current mirror circuit to a control signal input terminal of each of said plurality of second transistors,

wherein said voltage-to-current converter, said first and second current mirror circuits operate with a second power source voltage greater than the first power source voltage, and said ring oscillator and said third current mirror circuit operate with said first power source voltage.

2. A phase-locked loop apparatus as defined in Claim 1, wherein said voltage-to-current converter includes:

a transistor and resistor series circuit including a transistor and a resistor in series and configured to convert an input voltage into a current; and

an operational amplifier having a non-inverse terminal receiving said voltage output from said filter and an inverse terminal connected to an output terminal of said transistor of said transistor and resistor series circuit to form a negative feedback circuit, and configured to control an operation of said transistor of said transistor and resistor series circuit.

3. A phase-locked loop apparatus as defined in Claim 1, wherein said voltage-to-current converter includes a constant current source configured to supply a predetermined constant current to said first current mirror circuit.

4. A phase-locked loop apparatus as defined in Claim 1, wherein said third current mirror circuit includes a transistor with which each of said plurality of first transistors forms a current mirror circuit.

5. A phase-locked loop apparatus as defined in Claim 1, wherein said voltage-to-current converter includes a third transistor configured to form a current mirror circuit with each of said plurality of second transistors and to receive a current output from said third current mirror circuit.

6. A phase-locked loop apparatus, comprising:

a comparator configured to compare phases of a reference clock signal and an output signal of said apparatus and to output a voltage in accordance with a difference in phase as a comparison result;

a filter configured to integrate the voltage output from said comparator;

a voltage-controlled oscillator configured to control a frequency of an output signal in accordance with the voltage output from said filter, said voltage-controlled oscillator comprising:

a ring oscillator configured to include a delay circuit including a plurality of differential amplifiers connected in a ring form, each of said plurality of differential amplifier including a first transistor for controlling a current supplied to a corresponding one of said plurality of differential amplifiers by a first power source voltage and a second transistor for controlling a current output from a corresponding one of said plurality of differential amplifiers;

a voltage-to-current converter configured to convert said voltage output from said filter into a current;

a first current mirror circuit configured to output a current in accordance with the current output from said voltage-to-current converter;

a second current mirror circuit configured to output a current in accordance with the current output from said first current mirror circuit to a control signal input terminal of said first transistor included in each of said plurality of differential amplifiers; and

a third current mirror circuit configured to output a current in accordance with the current output from said second current mirror circuit to a control signal input terminal of said second transistor included in each of said plurality of differential amplifiers,

wherein said voltage-to-current converter, said first and second current mirror circuits operate with a second power source voltage greater than the first power source voltage, and said ring oscillator and said third current mirror circuit operate with said first power source voltage.

7. A phase-locked loop apparatus, comprising:

comparing means for comparing phases of a reference clock signal and an output signal of said apparatus and outputting a voltage in accordance with a difference in phase as a comparison result;

filtering means for integrating the voltage output from said comparing means;

voltage-controlled oscillating means for controlling a frequency of an output signal in accordance with the voltage output from said filtering means, said voltage-controlled oscillating means comprising:

ring oscillating means for delaying a signal with a plurality of inverting means connected in a ring form;

a plurality of first transistor means corresponding to said plurality of inverting means of said ring oscillating means on a one-to-one basis and controlling a current supplied by a first power source voltage to a positive side power source terminal of each of said plurality of inverting means;

a plurality of second transistor means corresponding to said plurality of inverting means of said ring oscillating means on a one-to-one basis and controlling a current output from a negative side power source terminal of each of said plurality of inverting means;

a voltage-to-current converting means for converting said voltage output from said filtering means into a current;

first current mirroring means for outputting a current in accordance with the current output from said voltage-to-current converting means;

second current mirroring means for outputting a current in accordance with the current output from said first current mirroring means to a control signal input terminal of each of said plurality of first transistor means; and

third current mirroring means for outputting a current in accordance with the current output from said second current mirroring means to a control signal input terminal of each of said plurality of second transistor means,

wherein said voltage-to-current converting means, said first and second current mirroring means operate with a second power source voltage greater than the first power source voltage, and said ring oscillating means and said third current mirroring means operate with said first power source voltage..

8. A phase-locked loop apparatus as defined in Claim 7, wherein said voltage-to-current converting means includes:

transistor and resistor series circuit means including a transistor and a resistor in series, for converting an input voltage into a current; and

operational amplifying means for controlling an operation of said transistor of said transistor and resistor series circuit means, having a non-inverse terminal receiving said voltage output from said filtering means and an inverse terminal connected to an output terminal of said transistor of said transistor and resistor series circuit means to form a negative feedback circuit.

9. A phase-locked loop apparatus as defined in Claim 7, wherein said voltage-to-current converting means includes constant current source means supplying a predetermined constant current to said first current mirroring means.

10. A phase-locked loop apparatus as defined in Claim 7, wherein said third current mirroring means includes a transistor with which each of said plurality of first transistor means forms a current mirror circuit.

11. A phase-locked loop apparatus as defined in Claim 7, wherein said voltage-to-current converting means includes third transistor means for forming a current mirror circuit with each of said plurality of second transistor means and receiving a current output from said third current mirroring means.

12. A phase-locked loop apparatus, comprising:

comparing means for comparing phases of a reference clock signal and an output signal of said apparatus and outputting a voltage in accordance with a difference in phase as a comparison result;

filtering means for integrating the voltage output from said comparing means;

voltage-controlled oscillating means for controlling a frequency of an output signal in accordance with the voltage output from said filtering means, said voltage-controlled oscillating means comprising:

ring oscillating means for delaying a signal, including a plurality of differential amplifying means connected in a ring form, each of said plurality of differential amplifying means including first transistor means for controlling a current supplied to a corresponding one of said plurality of differential amplifying means by a first power source voltage and second transistor means for controlling a current output from a corresponding one of said plurality of differential amplifying means;

voltage-to-current converting means for converting said voltage output from said filtering means into a current;

first current mirroring means for outputting a current in accordance with the current output from said voltage-to-current converting means;

second current mirroring means for outputting a current in accordance with the current output from said first current mirroring means to a control signal input terminal of said first transistor means included in each of said plurality of differential amplifying means; and

third current mirroring means for outputting a current in accordance with the current output from said second current mirroring means to a control signal input terminal of said second transistor means included in each of said plurality of differential amplifying means,

wherein said voltage-to-current converting means, said first and second current mirroring means operate with a second power source voltage greater than the first power source voltage, and said ring oscillating means and said third current mirroring means operate with said first power source voltage.

13. A method of phase-locked looping, comprising the steps of:

providing a ring oscillator including a plurality of inverters connected in a ring form;

comparing phases of a reference clock signal and an output signal of said apparatus;

generating a voltage in accordance with a difference in phase as a comparison result;

integrating the voltage output from said generating step;

converting said voltage output from said integrating step into a current;

first mirroring said current converted in said converting step to output a current in accordance with the current output from said converting step;

second mirroring said current output in said first mirroring step to output a first current in accordance with the current output in said first mirroring step; and

third mirroring said current output in said second mirroring step to output a second current in accordance with the current output from said second mirroring step,

first applying said first current output in said second mirroring step to a plurality of first transistors corresponding to said plurality of invertors of said ring oscillator on a one-to-one basis to control a current supplied by a first power source voltage to a positive side power source terminal of each of said plurality of invertors; and

second applying said second current output in said third mirroring step to a plurality of second transistors corresponding to said plurality of invertors of said ring oscillator on a one-to-one basis to control a current output from a negative side power source terminal of each of said plurality of invertors, wherein said converting step, said first and second mirroring steps operate with a second power source voltage greater than the first power source voltage, and said ring oscillator and said third mirroring step operate with said first power source voltage.

14. A method of phase-locked looping, comprising the steps of:

providing a ring oscillator including a plurality of differential amplifiers connected in a ring form, each of said plurality of differential amplifiers including first and second transistors;

comparing phases of a reference clock signal and an output signal of said apparatus;

generating a voltage in accordance with a difference in phase as a comparison result;

integrating the voltage output from said generating step;

converting said voltage output from said integrating step into a current;

first mirroring said current converted in said converting step to output a current in accordance with the current output from said converting step;

second mirroring said current output in said first mirroring step to output a first current in accordance with the current output in said first mirroring step; and

third mirroring said current output in said second mirroring step to output a second current in accordance with the current output from said second mirroring step,

applying said first current output in said second mirroring step to said first transistor included in each of said plurality of differential amplifiers of said ring oscillator to control a current supplied by a first power source voltage to each of said plurality of differential amplifiers; and

applying said second current output in said third mirroring step to said second transistor included in each of said plurality of differential amplifiers of said ring oscillator to control a current output from a negative side power source terminal of each of said plurality of differential amplifiers,

wherein said converting step, said first and second mirroring steps operate with a second power source voltage greater than the first power source voltage, and said ring oscillator and said third mirroring step operate with said first power source voltage.

15. A phase-lock loop comprising:

a first input for power at a first voltage and a second input for power at a second voltage that is higher than the first voltage;

a phase comparator, a charge pump, a loop filter, and a voltage controlled oscillator interconnected in a phase-lock loop configuration to maintain an output of the voltage controlled oscillator at a desired frequency;

said loop filter providing a voltage output as an input to said voltage controlled oscillator, and said voltage controlled oscillator in response providing said output thereof at a frequency related to said voltage input thereto from the loop filter;

said phase comparator receiving as inputs a clock signal and a signal related to said output of the voltage controlled oscillator, and providing to the charge pump, as an input thereto, a signal related to a phase relationship between said two inputs to the phase comparator;

said charge pump providing to the loop filter a signal related to the input thereto from the charge pump;

wherein said voltage controlled oscillator comprises:

a ring oscillator having an output coupled to provide said voltage controlled oscillator output at said desired frequency, said ring oscillator being powered through said input supplying power at said first voltage that is lower than said second voltage, and

other circuits coupled to receive said voltage output from said loop filter, said other circuits being powered through said second input supplying power at said second voltage that is higher than said first voltage;

said first and second voltage levels being selected to reduce a gain of said voltage controlled oscillator and thereby improve performance characteristics of said phase-lock loop relative to a gain at operating all of the voltage controlled oscillator at said second voltage.

16. A phase-lock loop as in claim 15 in which said voltage controlled oscillator comprises a bias current supplying circuit coupled between said loop filter and said ring oscillator to supply a bias current controlling said ring oscillator, said bias current supplying circuit comprising said other circuits that are powered through said second input supplying power at said second voltage that is higher than said first voltage.

17. A phase-lock loop as in claim 16 in which said bias current supplying circuit comprises a voltage-to-current converter and first, second and third current

mirror circuits, said voltage-to-current converter being configured to receive said voltage output of said loop filter, and said first and second current mirror circuits being functionally between said voltage-to-current converter and said third current mirror circuit, said voltage-to-current converter and said fist and second current mirror circuits comprising said other circuits that are powered through said second input supplying power at said second voltage that is higher than said first voltage, and said third current mirror circuit being functionally between said second current mirror circuit and said ring oscillator and being powered through said input supplying power at said first voltage that is lower than said second voltage.

18. A phase-lock loop as in claim 15 in which said ring oscillator comprises a plurality of inverter circuits connected in ring form.

19. A phase-lock loop as in claim 15 in which said ring oscillator comprises a plurality of differential amplifiers.

20. A method of providing a phase-lock output frequency comprising:

providing power at a first voltage and at a second voltage that is higher than the first voltage;

operating a voltage controlled oscillator in a phase-lock loop configuration with at least a phase comparator and a feedback frequency divider, including supplying the voltage controlled oscillator with an input voltage related to an output of the phase comparator and supplying the phase comparator with a clock signal and with a second input related to an output of the voltage controlled oscillator processed through said frequency divider;

powering a first portion of said voltage-controlled oscillator at said second voltage that is higher than said first voltage while powering a second portion of said voltage controlled oscillator at said first voltage that is lower than the second voltage to thereby improve performance of the phase-lock loop, including reducing jitter, compared to powering all of the voltage controlled oscillator at said second voltage;

said powering of said first portion including powering a voltage-to-current converter coupled to receive said voltage input related to said output of the phase comparator, and said powering of the second portion comprising powering at least a ring oscillator coupled to receive an input related to an output of said voltage-to current converter and to provide an output at a phase-locked frequency.

21. A method as in claim 19 wherein said powering of said first portion of said voltage controlled oscillator further comprises powering a first and a second current mirror circuits functionally coupled between said voltage-to-current converter and a third current mirror circuit, and said powering of a second portion further comprises powering said third current mirror circuit, wherein said third current mirror circuit is functionally coupled between the first and second current mirror circuits and said ring oscillator.